REMARKS/ARGUMENTS

Claims 10-15 were pending in the Application. By this Amendment, claim 10 is being amended and new claim 16 is being presented, to advance the prosecution of the Application. No new matter is involved.

On page 3 of the Office Action, claims 10-12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over newly cited U.S. patent 5,789,763 of Kato et al. According to the Office Action, Figure 2 of Kato teaches a plurality of semiconductor elements where the channel areas are arranged separately and in different directions to each other, and also teaches laser annealing. According to the Office Action, it would have been obvious to make all of the transistors in the column-driving circuits of Figure 2 of the same conductivity type, and it would have been obvious to provide electrical connections between the transistors in the column-driving circuits, because, as shown in Figure 9, the column-driving circuits must themselves be driven by addressing and other input circuits with interconnecting wiring.

On page 2 of the Office Action, claims 13-15 are rejected under 35 U.S.C. § 102(e) as being anticipated by Kato et al. Figure 6 of Kato et al. is said to show a plurality of semiconductor elements on a substrate in which each column includes a plurality of channel areas subject to laser annealing. All the pixels are said to be identical, so that all channels have the same conductivity type. Each channel in a given column is said to be electrically connected to the others, and each of the channels in a column is arranged separately and in parallel to each other. These rejections are respectfully traversed.

Kato et al. describes a substrate for a display device and a TFT display element using the substrate. A plurality of row electrode lines and a plurality of column electrode lines are arranged in a matrix form on the substrate. Pixel

electrodes and pixel-drive-TFTs each having a polycrystalline semiconductor channel are provided so as to correspond to each intersection of the row electrode lines and the column electrode lines. The pixel-drive-TFTs are arranged in a line-like form in the direction of the row electrode line. Row signals are supplied through the row electrode lines to the pixel-drive-TFTs. Column signals are supplied through the column electrode lines to the pixel-drive-TFTs. A plurality of row driver circuits for supplying row signals are formed on the substrate so as to correspond to each of the row electrode lines. Each of the row driver circuits has row-drive-TFTs. The row-drive-TFT has a polycrystalline semiconductor channel. The row-drive-TFT is arranged in a line-like form in the direction of row electrode line with respect to the pixel-drive-TFTs for a single row electrode line.

In applying Kato et al. to reject the claims, the Office Action notes that the semiconductor regions of TFTs are arranged in different directions, as shown for example in Figure 2 of the reference. The Office Action points out that in Kato et al., the channel areas are arranged separately and in different directions to each other.

Claim 10 defines a semiconductor device having a plurality of semiconductor elements on a substrate. Some or all of the semiconductor elements each has a plurality of channel areas (a) which are formed in a semiconductor layer subjected to laser annealing respectively, and (b) which are the same conductive type channel areas, and "the plurality of channel areas are electrically connected to each other and arranged separately and in different directions to each other". In this regard, the Office Action asserts that it would have been obvious to provide electrical connections between the transistors in the column-driving circuits, because the column-driving circuits must themselves be driven by addressing and other input circuits with interconnecting wiring. Therefore, according to the Office Action, claims 10-12 are obvious in view of Kato et al. While Applicants believe that claim

10 clearly distinguishes patentably over Kato in its present form, nevertheless Applicants are amending claim 10 to further recite that the plurality of channel areas "are connected in parallel to each other with respect to a current path". Nowhere does Kato et al. show, describe or suggest that in a TFT having channels which are connected in parallel to each other with respect to a current path, the channels are arranged separately and in different directions to each other. Kato et al. does not even recognize the need for such feature.

Aside from Figure 2 of Kato et al. which is referred to in the Office Action, none of the drawings of Kato et al. illustrate the feature that the channels of TFTs having completely different channel width directions are connected. Figure 2 of the reference only shows silicon islands which are considered to form different TFTs, respectively, and formed in different directions, and does not disclose or suggest that TFTs are formed in different directions and are connected to each other.

Applicants respectfully submits that the common knowledge of persons of ordinary skill in the art would lead them "not to unnecessarily connect" transistors, and the feature of connecting channels of TFTs arranged in different directions to each other, which is contrary to common knowledge is not described or suggested by Kato et al. The fact that Kato et al. does not suggest such feature is evidence that the reference does not recognize the necessity of connecting silicon islands arranged in different directions to each other. As previously described, Kato et al. has no description concerning the channels as recited in claim 10, and does not even describe the necessity of such connection and arrangement.

Again, claim 10 defines a semiconductor device in which the plurality of channel areas are electrically connected to each other and arranged separately and in different directions to each other. Additionally, and as amended herein, claim 10 defines the channel areas as "connected in parallel to each other with respect to a

current path". Therefore, claim 10 is submitted to clearly distinguish patentably over Kato et al.

Claims 11 and 12 depend from and contain all of the limitations of claim 10, so that such claims are also submitted to clearly distinguish patentably over the reference.

Regarding claims 13-15, the Office Action indicates that the pixel TFT of Kato et al. has a double gate structure, and that the channels of such TFT correspond to the channels recited in claim 13 which have the same conductivity type, are electrically connected to each other, and are arranged separately and in parallel to each other.

However, the channels recited in claim 13 are the channels within a driver circuit which are "electrically connected in parallel". More specifically, the channels are connected in parallel with respect to a current path. Although the channels of a double gate type TFT of Kato et al. (similar to the CMOS transistors in the driver section) are arranged in parallel with respect to the gate electrode, they are not "electrically connected in parallel", but are connected "electrically in series".

For the channels which are serially connected, when one of the channels becomes defective, the entire current path, including the other channels serially connected to the defective channel, also becomes defective. When a crystallization defective region is caused in the present invention, it is not possible to prevent deterioration of the characteristic of the entire current path. Namely, in essence, Kato et al. does not recognize the problems which are solved by the present invention, and such reference contains no description which could constitute a motivation for the present invention. Therefore, the present invention is neither anticipated by nor obvious from Kato et al.

Therefore, claim 13 is submitted to clearly distinguish patentably over Kato et al. in its present form. The claim defines a semiconductor device in which a

plurality of channel areas are electrically connected to each other and arranged separately and in parallel to each other.

Claim 14 depends from and further defines claim 13 in terms of a distance between the plurality of channel areas being determined that a virtual channel width containing a separated space is larger than a width of a defectively processed area caused in the semiconductor layer during the laser annealing. The Office Action indicates that a "virtual channel width" can be chosen to contain spaces that do not contain silicon at all so that the virtual channel width would be larger than any defective area of the silicon.

The "virtual channel width" of claim 14 contains "the channels which are electrically connected in parallel" with respect to each other and a region between these channels. However, it is common knowledge among those of ordinary skill in the art of semiconductor integrated circuits to attempt to increase the degree of integration of the circuit elements and to try to match the characteristics of the elements which operate in the same manner by forming those elements as closely to each other as possible. In view of this, it is a concept completely contrary to the common knowledge of those of ordinary skill in the art to physically "separate" the channels which are electrically connected in parallel and to make the virtual channel width including the separated space larger than the width of the defectively processed area, namely to actively increase the physically separated space. Nothing in Kato et al. describes or suggests any recognition for the motivation of the present invention. Therefore, claim 14 is submitted to clearly distinguish patentably over Kato et al.

Claim 15 depends from and contains all of the limitation of claim 13. Therefore, claim 15 also clearly distinguishes patentably over the art.

New claim 16 depends from and further defines claim 13 in terms of "the channel areas are connected in parallel with respect to a current path" much in the

same manner that claim 10 has been amended to recite such feature. Therefore, claim 16 is submitted to clearly distinguish patentably over Kato et al.

In conclusion, claims 10-16 are submitted to clearly distinguish patentably over the cited reference for the reasons described above. Therefore, reconsideration and allowance are respectfully requested.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6846 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: August 8, 2003

By: _____
John P. Scherlacher
Registration No. 23,009
Attorney for Applicant(s)

500 South Grand Avenue, Suite 1900
Los Angeles, California 90071
Phone: 213-337-6700
Fax: 213-337-6701